REMARKS

This amendment is responsive to a final Office Action mailed September 6, 2006 ("Office Action").

The Office Action objected to FIGURE 13 for not having been labeled as prior art. The Office Action also objected to Claim 8 for informalities. The Office Action rejected Claims 8, 10, and 14 under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al., U.S. Patent Application Publication No. 2003/0188241 ("Zyuban et al."), in view of Woods et al., U.S. Patent Application Publication No. 2002/0162037 ("Woods et al."), in view of the applicants' admitted prior art disclosure in the application pages 1-6 (hereinafter "APA"), and further in view of Purdham, U.S. Patent No. 5,701,313 ("Purdham"). The Office Action further rejected Claims 9 and 11 under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al., in view of Woods et al., in view of APA, and in view of Purdham, and further in view of Freeman et al., U.S. Patent No. 6,510,528 ("Freeman et al."). The Office Action further rejected Claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al., in view of Woods et al., in view of APA, and in view of Purdham, and further in view of Smith III, U.S. Patent No. 5,502,728 ("Smith III"). The Office Action further rejected Claim 13 under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al., in view of Woods et al., in view of APA, and in view of Purdham, and further in view of Broseghini et al., U.S. Patent No. 5,761,489 ("Broseghini et al.").

Claims 12-14 have been canceled without prejudice. Claims 8-11 have been amended to further clarify claim language.

Applicants have carefully considered each of the cited references and the remarks made in the Office Action and submit that the amended claims presented above are in patentable

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condition. Reconsideration of the application and allowance of the claims at an early date is respectfully requested.

Objection to the Drawings

As noted above, the Office Action objected to FIGURE 13 for not having been labeled as prior art. A replacement sheet for FIGURE 13 is attached as a replacement drawing. Accordingly, applicants respectfully request the objection to the drawings be withdrawn.

Claim Objections

As noted above, the Office Action objected to Claim 8 because of informalities. Claim 8 has been amended to correct the informalities. Accordingly, applicants respectfully request the objection to Claim 8 be withdrawn.

Rejection of Claims 8, 10, and 14 Under 35 U.S.C. § 103(a)

As noted above, Claims 8, 10, and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al., in view of Woods et al., in view of APA, and further in view of Purdham. As noted above, Claim 14 has been canceled without prejudice, thus rendering the rejection moot.

Amended Claim 8 recites, *inter alia*, "a shift register including a *plurality of flipflops* connected to the scan chain, wherein the shift register stores the save data output . . . by the *shift operation* . . . and . . . *error checking and correction* for the save *data stored in the shift register* . . ., wherein the number of the shift operations equals the number of the flipflops of the functional module." Zyuban et al. does not teach or suggest a *shift register including a plurality of flipflops*, as recited by amended Claim 8. Zyuban et al. discloses a circuit having a latch 60 with date retention capability (¶ 0023). Zyuban et al. discloses that the latch 60 is provided with a data path 22 for restoring *the data* from the latch 60 to the main flip-flop 50 (¶ 0023). Figure 5 of Zyuban et al. clearly shows that a *single bit* of data from the flip-flop 50 may be stored and

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restored by the latch 60. Figure 5 discloses a one-to-one direct connection between the latch 60 and the flip-flop 50. This is in contrast to a shift register including a plurality of flip-flops connected to the scan chain storing data by shift operations. Those skilled in the art will appreciate that a multi-bit shift register contains *multiple bits* of data wherein the *individual bits are not directly connected* to the source of data, but rather, the data bits are stored into the shift register one at a time by a shift operation. Additionally, Zyuban et al. does not teach or suggest error checking and correction ("ECC") for the data stored in the shift register, as recited in amended Claim 8. Those skilled in the art will appreciate that ECC can only be generated for multiple bits of data. Therefore, the circuit disclosed by Zyuban et al. is fundamentally not capable of providing ECC for the single bit of data stored in latch 60.

Woods et al. fails to supply the teachings missing from Zyuban et al., namely, a plurality of flip-flops connected to the scan chain and ECC for the data stored in the shift register. Woods et al. does not teach or suggest a shift register connected to the scan shift wherein the shift register stores the save data output from the functional module. Woods et al. discloses a memory unit 270 for use in storing state information (¶ 0057). Woods et al. further discloses that "the memory 270 is preferably a nonvolatile memory (e.g., an *EEPROM*) so that the information stored therein is retained during periods of inactivity." Woods et al. further discloses that the memory 270 can be a volatile memory (e.g., a random access memory (*RAM*)). (emphasis added; ¶ 0057.) Woods et al. further discloses that in state D_5, the ISPRFSM 260 checks *the address counter* against a value . . . the address counter reaches when all the data in the FFs has been stored in the *RAM* (¶ 0084). Those skilled in the art will appreciate that an address counter, RAM, and EEPROM are memory components used in memory modules that include randomly addressable binary words and wherein data is read and written *in parallel* (i.e., multiple bits at a time). This is in contrast to the *shift register, which is a serially accessed memory component, as*

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recited in amended independent Claim 8. Those skilled in the art appreciate that the shift operation is inherently a serial bit transfer operation.

The APA and Purdham references fail to supply the teachings missing from Zyuban et al. and Woods et al., namely, a plurality of flip-flops connected to the scan chain and ECC for the data stored in the shift register. The APA indicates the use of discrete flip-flops FF1 and FF2, FRAM, DRAM and high voltages on memory modules as a means of preventing occurrence of soft errors (pp. 3-6). The APA does not teach or suggest the use of a shift register and ECC. Purdham discloses the use of RAM 20 and ECC on parallel, word addressable, multi-bit memory performed one or more words at a time, in contrast to ECC performed when the save data is to be restored *by the shift operation using the scan chain*, as recited by Claim 8. Therefore, amended Claim 8 is submitted to be allowable for at least the reasons discussed above.

Rejection of Claims 9 and 11 Under 35 U.S.C. § 103(a)

As noted above, Claims 9 and 11 were rejected by the Office Action under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al., in view of Woods et al., in view of APA, in view of Purdham, and further in view of Freeman et al.

Claim 9 depends from amended Claim 8 and is submitted to be allowable for at least the same reasons presented above with respect to Claim 8. Freeman et al. fails to supply the teachings missing from Zyuban et al., Woods et al., APA, and Purdham, namely, a plurality of flip-flops connected to the scan chain and ECC for the data stored in the shift register. Freeman et al. does not teach or suggest a shift register and *ECC for the data stored in the shift register connected to the scan chain*, as recited in amended Claim 8. Freeman et al. discloses a memory scrubbing routine that is initiated by a periodic system wake-up scheme. The memory scrubbing routine reads out all memory locations for correction of single-bit ECC errors (Col. 2, lines 25-35). It is unclear how the flow diagram of Figure 2 discloses a shift register. Those

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skilled in the art will appreciate that general system memory in a computer system is *random access (RAM)*, as also signified by the phrase "memory locations" indicating randomly accessible memory. This is *in contrast to a shift register that is inherently a sequentially accessed device*. Therefore, Claim 9 is submitted to be allowable for these additional reasons.

Claim 11 depends from amended Claim 8, and is submitted to be allowable for at least the same reasons presented above with respect to Claim 8.

Rejection of Claim 12 Under 35 U.S.C. § 103(a)

As noted above, the Office Action rejected Claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al., in view of Woods et al., in view of APA, and in view of Purdham, and further in view of Smith III. Also, as noted above, Claim 12 has been canceled without prejudice, thus rendering the rejection moot.

Rejection of Claim 13 Under 35 U.S.C. § 103(a)

As noted above, the Office Action rejected Claim 13 under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al., in view of Woods et al., in view of APA, and in view of Purdham, and further in view of Broseghini et al. Also, as noted above, Claim 13 has been canceled without prejudice, thus rendering the rejection moot.

CONCLUSION

For the reasons set forth above, applicants respectfully submit that all of the rejection claims remaining in this application are clearly allowable in view of the cited and applied

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references, singly or in any motivated combination. As a result, early and favorable action allowing these claims and passing this application to issue are respectfully solicited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first-class mail with postage thereon fully prepaid and addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date.

Date: Jan. 8, 2007 Patricia Gubble

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